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MICHAEL J MALLIE
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
ELMORE, REBA I	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 19

Application Number: 09/205,086
Filing Date: December 04, 1998
Appellant(s): BOGIN et al.

Mark L. Watson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 15, 2002

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

This appeal involves claims 1-28 and 38-49

(4) Status of Amendments After Final

The amendment after final rejection filed on May 31, 2002 has been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is not correct. The changes are as follows: claims 1-5, 16-19 and 38-40 are rejected as being clearly anticipated by a Direct Rambus Technology Disclosure under 35 USC 102(b). Claims 6-15, 20-28 and 41-49 are

rejected as being unpatentable over a Direct Rambus Technology Disclosure under 35 USC 103(a).

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-28 and 38-49 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

Direct Rambus Technology Disclosure October 15, 1997 by Rambus, Inc.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 16-19 and 38-40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by a **Direct Rambus Technology Disclosure**.

The Direct Rambus Technology Disclosure teaches the invention (claims 1-3, 16-17 and 38) as claimed including a timing circuit in a memory controller within a computer system, with the controller comprising:

a memory which is taught as RDRAMS (e.g., see Figure 2);

a memory controller which includes a refresh timing circuit for generating clock pulses used to trigger memory refreshes (e.g., see Figure 2 and the section titled 'Features of the Rambus Memory Controller' on page 14);

the internal clock generator is taught as part of the chip level device (e.g., see the section titled 'The Physical Layer' on page 8); and,

the counters, storage registers and the comparators used for the refresh timing circuit are all common elements which are necessary for such a device to perform its basic functions and are considered inherent to the controller.

As to claim 2, the reference teaches the refresh timing circuit for triggering refresh timing events (e.g., see Figure 4 and the section titled 'Signals' on page 8).

As to claims 4, 19, and 40, the reference inherently teaches a counter for counting the number of clock pulses generated by the clock generator since counters are necessary elements of a controller which performs functions based on clock signals. Refreshes must be performed by specific intervals for any type of DRAM or else the contents are no longer viable.

As to claims 5, 18, and 39, the reference teaches four modes of operation, Nap, Standby, PwrDown and Active. For all of these modes of operation refreshes must be done by a set time frame for the data to be reliable for any type of DRAM.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-15, 20-28 and 41-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over a **Direct Rambus Technology Disclosure**.

The independent claims and intervening claims are taught as given above in the rejection under 35 USC 102(b).

As to claims 6, 20 and 41, the reference does not specifically teach the storage register transmitting the data to the comparator upon a transition from a normal mode to a low power mode. However, the reference does teach a normal mode and a low power mode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the circuitry include storage registers and comparators for use in going from a normal mode to a low power mode as these are common and necessary elements for use with this type of functionality and circuitry.

As to claims 7, 21-23 and 42-44, the reference inherently teaches a first counter transmitting signals to the comparator whenever the computer system is operating in a low power mode with the signal representing the number of clock pulses received from the clock generator. Even in the low power mode the DRAM must be refreshed by a set number of clock pulses or else the data loses its integrity and is no longer usable.

As to claim 8, the reference inherently teaches transmitting a refresh trigger signal based on the circuitry reaching a specific number of clock pulses.

As to claims 9, 24 and 45, the reference does not specifically teach the refresh timing circuit comprising a second counter, however, counters are notoriously well known in the art and official notice is taken thereof. The claims are not stating a specific connectivity of the various components or elements, only that these components or elements are being used in the circuitry, however, these uses are the well known common applications of these components or elements.

As to claims 10-11, 25-26 and 46-47, the reference teaches both a normal mode and a low power mode of operation. In order for the system to maintain the refresh functions necessary, the clock pulses must be counted for each mode of operation. Without maintaining a count of the clock pulses, the DRAM cannot be refreshed before the integrity of the data is lost or unnecessary refreshes would occur which would impact the efficiency of the system.

As to claims 12-14, 27-28 and 48-49, the reference does not specifically teach a second counter being deactivated and a first counter being activated whenever the computer system transitions from a normal mode to a low power mode, however, performing refreshes to the RDRAM is taught in all the four modes of operation of the system which means counters must be used to keep track of the clock pulses for all four modes in order to perform the refreshes within the proper intervals. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use counters for counting the clock pulses in the timing circuitry for refreshes because the refreshes are performed during all four modes of operation and counters are common and necessary elements for refresh circuitry and official notice is taken thereof.

As to claim 15, the reference discloses the claimed invention except for the memory being comprised of Extended Data Out Dynamic Random Access Memory (EDO DRAM) and the memory controller therefore being a EDO DRAM controller. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use EDO DRAM because it

has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious choice (*In re Leshin,* 125 USPQ 416).

(11) Response to Argument

As to the remarks concerning the reference not teaching a refresh timing circuit for generating clock pulses used to trigger memory refreshes, it is true that the reference does not go into an in depth discussion concerning the refresh operation. However, the Rambus memory controller (RMC) is a controller for dynamic RAM (DRAM) which inherently requires refreshing in order to maintain coherency of the stored data. On page 14 of the reference it is states that the RMC supports all control functions including protocol, refresh memory and interleaving support. In order to support refresh functions clock pulses must be used to trigger memory refreshes necessary for DRAM. It is admitted that there is not a great deal of details given in relationship to the refresh functions, however, the independent claims are substantially broad and are taught to the extent required by the actual claim language. DRAM refreshes must be triggered and the triggering mechanism is controlled by the RMC. The fact that the reference does not state the words that 'a refresh timing circuit for generating clock pulses used to trigger memory refreshes' in the given reference but that does not indicate that the RMC does not perform this functionality. In fact, this function must take place otherwise the DRAM would be unreliable and useless and this is again given on page 10 where it is stated 'Other commands can be sent across the row pins, including refresh and power state control.'

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Reba I. Elmore
Primary Patent Examiner

November 14, 2002

Conferees

David Robertson
Primary Patent Examiner

Do H. Yoo
Supervisory Patent Examiner

Mark L. Watson
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
7TH FLOOR
LOS ANGELES, CA 90025